an MPEG Transport processor for receiving a plurality of MPEG Transport streams, at least one of the MPEG Transport streams including MPEG video data;

an MPEG video decoder for processing the MPEG video data to generate video for displaying;

means for displaying the video; and

a system bridge controller for coupling a CPU to at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and to a plurality of peripheral devices,

wherein the system bridge controller performs format conversion between big-endian data and little-endian data, between the CPU and at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and between the CPU and one or more of the plurality of peripheral devices.

42. The system of claim 41 wherein the MPEG Transport processor, the MPEG video decoder, the means for displaying the video and the system bridge controller are integrated on an integrated circuit chip.

43. The system of claim 41 wherein the MPEG video data include HDTV video data.

44. The system of claim 41 wherein the MPEG video data include SDTV video data.

REMARKS

The "Amendment" mailed September 17, 2001 has been canceled because it has been erroneously titled as an Amendment even though no amendment has been made to the application. Further, the September 17, 2001 response did not address the objection to Oath/Declaration under 37 C.F.R. § 1.52(c).

Applicants appreciate the Examiner's time and the opportunity afforded to the Applicants' attorney during the telephone interview on September 12, 2001 during which the Examiner requested that the arguments be submitted in writing.

The Examiner has indicated that formal drawings will be required when the application is allowed. Applicants acknowledge and will file the formal drawings when the application is allowed.

The Examiner has objected to the Oath/Declaration under 37 C.F.R. § 1.52(c). Please find enclosed a copy of the Response to Missing Parts with the executed Declaration.

Claims 1-44 remain in the present application. None of the claims has been amended. In view of the following remarks, Applicants respectfully request reconsideration and allowance of claims 1-44.

In various different embodiments of the present invention, a video and graphics system preferably includes a system bridge controller, which is used to couple a CPU to peripheral devices. The system bridge controller preferably provides interfaces between I/O devices, the PCI bus, system memory, and the CPU. The system bridge controller may be integrated on the same integrated circuit chip as the video and graphics system (e.g., page 2, lines 26-31; page 184, lines 4-18).

The Examiner has rejected claims 1-44 under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,982,459 issued to Fandrianto et al.("Fandrianto"). The Examiner alleges that "Fandrianto teaches a host interface having the same functionality as a system bridge controller. The host interface transmits compressed video data to a host bus, a local bus, computer system, and any other peripheral devices," and cites col. 1, lines 38-46 and col. 3, lines 40-61 of Fandrianto.

However, Fandrianto on col. 1, lines 42-44 recites that "the universal multimedia computer communications processor is fabricated on a single integrated circuit chip" without any reference to a system

bridge controller. Further, Fandrianto on col. 3, lines 52-54 recites that "[h]ost interface 214 is for connection of a host device such as a host processor (not shown) in a personal computer system" with no indication that this host interface is going to be used for interfacing the host device with anything but the communications processor (i.e., VCP). In these and other sections of Fandrianto, Applicants are unable to find any disclosure that explains how or why the host interface can be considered to have the same functionality as the system bridge controller of the present application.

Instead, Fandrianto appears to disclose a video communications processor (VCP), which is a single-chip programmable video codec and multimedia communication processor that has a host interface for communicating with a PC over PC bus interface and PC bus (col. 2, lines 63-66; col. 3, lines 52-54; FIG. 1). Further, the Examiner appears to argue that the "host interface," which the Examiner appears to equate to the "system bridge controller" of the present application, is on a single integrated circuit chip with the VCP. This assertion, however, is supported by neither the drawings nor the specification of Fandrianto.

For example, on col. 2, line 66 through col. 3, line 1, Fandrianto recites "[t]he VCP requires only memory and interface circuits for implementation of a complete multimedia and conferencing system." It is apparent from this passage that the interface circuits are not a part of the single-chip on which the VCP resides. Further, this interpretation is supported by FIG. 1 of Fadrianto where the VCP is connected to PC bus 118 over a host bus 114 and an external PC bus interface 186. As such, the VCP of Fandrianto appears to require the external PC bus interface 186 to connect to a host processor in a personal computer system, and does not appear to include integrated host interface circuitry.

As discussed above, even assuming that Fandrianto discloses a host interface integrated on a single-chip with the VCP, the host

interface is used to connect the VCP to a host processor (col. 3, lines 52-54). This is distinguishable from the system bridge controller of the present invention, which is used to couple a CPU to a plurality of peripheral devices, such as, for example, I/O devices and PCI devices.

Consider now the claims.

Claim 1 recites "[a] system on an integrated circuit chip comprising: an MPEG video decoder for processing MPEG video data to generate video for displaying; means for displaying the video; and a system bridge controller for coupling a CPU to a plurality of peripheral devices." Since Fandrianto neither teaches nor suggests "a system bridge controller for coupling a CPU to a plurality of peripheral devices," Applicants respectfully submit that claim 1 is not made unpatentable by Fandrianto. Therefore, Applicants respectfully request the rejection to claim 1 be withdrawn and that claim 1 be allowed.

Since claims 2-21 depend, either directly or indirectly, from claim 1, they incorporate all the terms and limitations of claim 1 and any intervening claims, in addition to other limitations, which together patentably distinguish them over the cited references. Therefore, Applicants respectfully request that the rejection to claims 2-21 be withdrawn as well, and that they be allowed.

Claim 22 recites "[a] method of coupling a CPU to other devices comprising the steps of: coupling the CPU to a plurality of peripheral devices via a system bridge controller on an integrated circuit chip, wherein the integrated circuit chip is used to process MPEG video data to generate video for displaying and to display the video." Since Fandrianto neither teaches nor suggests "coupling the CPU to a plurality of peripheral devices via a system bridge controller on an integrated circuit chip," Applicants respectfully submit that claim 22 is not made unpatentable by Fandrianto. Therefore, Applicants

respectfully request the rejection to claim 22 be withdrawn and that claim 22 be allowed.

Since claims 23-40 depend, either directly or indirectly, from claim 22, they incorporate all the terms and limitations of claim 22 and any intervening claims, in addition to other limitations, which together patentably distinguish them over the cited references. Therefore, Applicants respectfully request that the rejection to claims 23-40 be withdrawn as well, and that they be allowed.

Claim 41 recites, in relevant portion, "[a] system comprising: an MPEG Transport processor . . .; an MPEG video decoder . . .; means for displaying the video; and a system bridge controller for coupling a CPU to at least one of the MPEG Transport processor, the MPEG video decoder and the means for displaying the video, and to a plurality of peripheral devices . . ." Since Fandrianto neither teaches nor suggests "a system bridge controller for coupling a CPU to . . . a plurality of peripheral devices," Applicants respectfully submit that claim 41 is not made unpatentable by Fandrianto. Therefore, Applicants respectfully request the rejection to claim 41 be withdrawn and that claim 41 be allowed.

Since claims 42-44 depend directly from claim 41, they incorporate all the terms and limitations of claim 41, in addition to other limitations, which together patentably distinguish them over the cited references. Therefore, Applicants respectfully request that the rejection to claims 41-44 be withdrawn as well, and that they be allowed.

In view of the foregoing remarks, Applicants respectfully request allowance of claims 1-44. If the Examiner believes that another telephone conference with Applicants' attorney might expedite prosecution of the application, the Examiner is invited to call at the telephone number indicated below.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____
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Reg. No. 43,693
626/795-9900

JEJ/sd
Enclosure: Letter in Response to
Notice to File Missing Parts of
Application mailed March 7, 2001.

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